REMARKS

Claims 1-35 are pending. Claims 12-16 were amended to address the outstanding claim objection. For at least the reasons set forth below, withdrawal of all outstanding rejections is respectfully requested.

Entry of Rule 116 Response

Entry of this response is requested because such response does not raise any new issues that would require further consideration and/or search. No new matter is raised by this response. The amendments to claim 12 were previously discussed and approved by the Examiner.

It is requested that this response be entered even if the application is not allowed because this response will place the application in better form for appeal by materially simplifying the issues.

If the application is not in proper form for allowance, Applicants request that the Examiner telephone the undersigned to discuss any further outstanding issues.

Request for Interview Prior to Formal Action on Amendment

Applicants request an interview prior to formal action on this response. An "Applicant Initiated Interview Request Form" accompanies this response. Please contact Applicants' undersigned representative to schedule the interview.

Claim Objections

Claim 12 was amended to address the claim objection. Claims 13-16 were amended to conform these claims to claim 12. The claim amendments were previously presented to, and approved by, the Examiner in a telephone conversation held on November 22, 2005.

Prior Art Rejections

Claims 1-6, 10, 12-15, 17-23, 28-29 and 35[1] were rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Chen et al., hereafter, "Chen."

Claims 9, 26, 27, 31, 32, 33 and 35 were rejected under 35 U.S.C. § 103(a), as allegedly being unpatentable over Chen.

Claims 7, 8, 24, and 25 were rejected under 35 U.S.C. § 103(a), as allegedly being unpatentable over Chen et al. in view of Ker et al.

Claims 11, 16, and 30 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chen et al. in view of Consiglio.

Claim 34 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chen et al. in view of Barth et al.

Applicants respectfully traverse all of the above rejections.

1. Examiner's Response to Arguments in Final Rejection

In Applicants' previous response, it was argued that Chen's biasing source does not generate ESD-scale pulses, and actually outputs voltage levels that are orders of magnitude lower than typical ESD-scale levels. Thus, Chen's biasing source has nothing whatsoever to do with generating ESD-scale pulses. In response, the Examiner asserts that the specification does not disclose that an ESD-scale pulse is at a certain voltage, and that given the broadest possible interpretation, Chen's bias source of .1V or 1.1V could broadly be considered an ESD scale pulse. Applicants disagree that one of ordinary skill in the art would consider Chen's bias source to be an ESD-scale level, and thus Applicants repeat these arguments.

Notwithstanding this position, Applicants further assert that the Chen's bias source inherently cannot be an ESD-scale pulse because it is not a pulse signal, as discussed below.

[1] The Office Action also states that claims 31 and 32 are rejected on this basis. However this appears to be an error since claims 31 and 32 are rejected in section 5 of the Office Action under 35 U.S.C. § 103(a) and are specifically discussed in that section.

2. Patentability of independent claims 1, 12 and 18 over Chen

Claims 1, 12, 18 and 31 each recite at least the following underlined limitations that are not disclosed or suggested by Chen:

1. A system for measuring electrostatic discharge (ESD) characteristics of a semiconductor device, comprising:
at least one pulse generator generating ESD-scale pulses;
a first point of the semiconductor device receiving a first ESD-scale pulse from the at least one pulse generator;
a second point of the semiconductor device receiving the first ESD-scale pulse from the at least one pulse generator;
at least a third point of the semiconductor device receiving a second ESD-scale pulse from the at least one pulse generator;
and a data collector to collect data on the ESD characteristics of the semiconductor device.

12. A system for measuring electrostatic discharge (ESD) characteristics of a multi-terminal device, comprising:
a pulse generator including:
means for generating a first pulse, the first pulse providing a first ESD-scale pulse;
means for generating a second pulse, the second pulse providing a second ESD-scale pulse;
a first terminal of the multi-terminal device coupled to the means for generating a first pulse to receive the first ESD-scale pulse;
a second terminal of the multi-terminal device coupled to the means for generating a first pulse to receive the first ESD-scale pulse;
a third terminal of the multi-terminal device coupled to the means for generating a second pulse to receive the second ESD-scale pulse; and
a detector to detect a leakage current of the multi-terminal device, wherein the ESD characteristics of the multi-terminal device are determined when the detector detects a leakage current in the multi-terminal device.

18. A method of measuring electrostatic discharge (ESD) characteristics of a semiconductor device, comprising:
providing at least one pulse generator generating ESD-scale signals;
identifying a first point on the semiconductor device;
identifying a second point on the semiconductor device;
identifying a third point on the semiconductor device;
providing a first ESD-scale signal to the first and second points of the semiconductor device; and

providing a second ESD-scale signal to at least the third point on the semiconductor device.

In the outstanding rejection, the Examiner states that the claimed "third point" and "third terminal" that receives a "second ESD-scale pulse" is met by Figs. 13 and 14 of Chen, particularly, a "biasing source generating a pulse into the gate." See page 3, lines 3-6 of the Office Action. Applicants respectfully disagree with this statement. In fact, Chen's biasing source (V_G) does not generate an ESD-scale pulse or even a non-ESD-scale pulse because Chen's biasing source (V_G) is a fixed (constant) power source. A fixed (constant) power source inherently cannot be a pulse or a pulse generator. In electronics, a "pulse" is a current or voltage which changes abruptly from one value to another and back to the original value in a finite length of time.

Accordingly, the basis for the rejection of claims 1, 12 and 18 is improper, even if Chen's bias source is considered to be an ESD-scale level signal as asserted by the Examiner. Claims 1, 12 and 18 are thus believed to be patentable over Chen.

3. Patentability of independent claim 31 over Chen

Claim 31 recites at least the following underlined limitations that are not disclosed or suggested by Chen:

31. A method of electrostatic discharge (ESD) testing, comprising:
providing a multi-terminal semiconductor device;
generating at least two ESD-scale pulses;
providing a first ESD-scale pulse of the at least two ESD-scale pulses to a first and a second terminal of the multi-terminal device;
providing a second ESD-scale pulse of the at least two ESD-scale pulses to at least the second terminal and a third terminal of the multi-terminal device;
collecting ESD characteristics of the multi-terminal device under the first and second ESD-scale pulses; and
detecting if a leakage current flows in the multi-terminal semiconductor device.

Claim 31 is believed to be patentable for at least the same reason as given above for claims 1, 12 and 18.

Furthermore, the Examiner states that the claimed "third terminal" is met by one of the four points connected to the drain, as shown in Fig. 4 of Chen. See page 5, lines 7-16 of the Office Action. (The other end of these four points are connected to an ESD source.) However, claim 31 explicitly recites a "multi-terminal semiconductor device," and thus the claimed "third terminal" inherently must be connected to a physically separate terminal of the semiconductor device. In contrast to the claimed invention, in Chen, all of the points are physically connected to the same terminal of a semiconductor device, namely the drain.

For at least these reasons, the basis for the rejection of claim 31 is improper, even if Chen's bias source is considered to be an ESD-scale level signal as asserted by the Examiner. Claim 31 is thus believed to be patentable over Chen.

4. Patentability of dependent claims

The dependent claims are believed to be patentable over the applied references for at least the reason that they are dependent upon allowable base claims and because they recite additional patentable elements and steps.

Nor do Ker, Consiglio or Berth make up for the deficiencies highlighted in Chen above.

Conclusion

Insofar as the Examiner's rejections were fully addressed, the present application is in condition for allowance. Issuance of a Notice of Allowability of all pending claims is therefore requested.

Respectfully submitted,

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